	Applicati n No.	Applicant(s)
Notice of Allowability	09/717,570	THOMPSON, CAROL L.
	Examiner	Art Unit	
	Tuan A Vu	2124	

-- Th MAILING DATE of this communication appears on the cov r sheet with the correspond nce address--

All claims b ing allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included her with (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *8/20/2004*.

2. ☒ The allowed claim(s) is/are *1-15*.

3. ☒ The drawings filed on *21 November 2000* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some*   c)☐ None   of the:

       1. ☐ Certified copies of the priority documents have been received.

       2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

       3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

    * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.

    (a)☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached

       1)☐ hereto or 2)☐ to Paper No./Mail Date _____ .

    (b)☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachm nt(s)

1. ☐ Notice of References Cited (PTO-892)

2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____

4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

5. ☐ Notice of Informal Patent Application (PTO-152)

6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .

7. ☒ Examiner's Amendment/Comment

8. ☒ Examiner's Statement of Reasons for Allowance

9. ☐ Other _____ .

DETAILED ACTION

1.   This action is responsive to the Applicant's response filed 8/20/2004.

As indicated in Applicant's response, claims 1-15 are re-submitted and are pending in the

office action.

EXAMINER'S AMENDMENT

2.   An examiner's amendment to the record appears below. Should the changes and/or

additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR

1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the

payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with

attorney Robert Blaha, Reg # 43502 on 12/17/2004.

The application has been amended as follows:

Claim 1:

An apparatus for performing correctness checks, the apparatus comprising:

logic configured to receive a first set of instructions <u>comprising one or more conditional

code sequences that when executed direct one or more correctness checks</u>;

logic configured to generate an initial instruction schedule and a conditional

instruction stream from the first set of instructions, such that the initial instruction

schedule is devoid of <u>said conditional</u> code sequences ~~comprising correctness check functions~~

and such that <u>the conditional</u> code sequences of the conditional instruction stream are associated

with a corresponding set of one or more instructions in the initial instruction schedule;

logic configured to evaluate the initial instruction schedule to determine whether the

initial instruction schedule includes spare instruction slots into which said <u>conditional</u> code

sequences ~~associated with correctness check functions~~ can be inserted into the initial instruction

schedule such that a final instruction schedule ~~responsive to the initial instruction schedule~~

would not require a longer run time than the initial instruction schedule; and

logic configured to generate the final instruction schedule responsive to the

initial instruction schedule, the conditional instruction stream, and the logic

configured to evaluate <u>such that identified conditional code sequences are inserted into spare</u>

<u>instruction slots</u>.

Claim 2:

The apparatus of claim 1, wherein correctness check<u>s</u> ~~functions~~ are configured to

evaluate at least one of a value, a range of values, and a relationship between values after

execution of the corresponding instructions in the initial instruction schedule.

Claim 4:

An apparatus for performing correctness checks, the apparatus comprising:

means for receiving a first set of instructions <u>comprising one or more conditional code</u>

<u>sequences that when executed direct one or more correctness checks</u>;

means for generating an initial instruction schedule and a conditional instruction stream

from the first set of instructions, such that the initial instruction schedule is devoid of <u>said</u>

<u>conditional</u> code sequences ~~comprising correctness check functions~~ and such that code sequences

of the conditional instruction stream are associated with a corresponding set of one or more

instructions in the initial instruction schedule;

means for evaluating the initial instruction schedule to determine whether the initial

instruction schedule includes spare instruction slots into which said <u>conditional</u> code sequences

~~associated with correctness-check functions~~ can be inserted into the initial instruction schedule

such that a final instruction schedule would not require a longer time than the initial instruction

schedule; and

means for inserting said <u>conditional</u> code sequences ~~associated with the correctness check
function~~ into the spare instruction slots <u>to generate the final instruction schedule</u> if enough spare

instruction slots exist in the initial instruction schedule ~~for accommodating~~ <u>to accommodate</u> said

<u>conditional</u> code sequences.

Claim 5:

The apparatus of claim 4, wherein correctness check<u>s</u> ~~functions~~ are configured to

evaluate at least one of a value, a range of values, and a relationship between values after

execution of the corresponding instructions in the initial instruction schedule.

Claim 6:

A method for performing correctness checks, the apparatus comprising:

receiving a first set of instructions <u>comprising one or more conditional code sequences</u>

<u>that when executed direct one or more correctness checks</u>;

generating an initial instruction schedule and a conditional instruction stream from the

first set of instructions, such that the initial instruction schedule is devoid of <u>said conditional</u>

code sequences ~~comprising correctness-check functions~~ and such that code sequences of the

conditional instruction stream are associated with a corresponding set of one or more instructions

in the initial instruction schedule;

evaluating the initial instruction schedule to determine whether the initial instruction schedule includes spare instruction slots into which said <u>conditional</u> code sequences from the conditional instruction stream ~~and associated with correctness check functions~~ can be inserted into the initial instruction schedule such that a final instruction schedule would not require a longer time than the initial instruction schedule; and

inserting said <u>conditional</u> code sequences ~~associated with the correctness check function~~ into the spare instruction slots <u>to generate the final instruction schedule</u> ~~if~~ <u>when</u> enough spare instruction slots exist in the initial instruction schedule ~~for accommodating~~ <u>to accommodate</u> said <u>conditional</u> code sequences.

Claim 7:

The method of claim 6, wherein evaluating the initial instruction schedule comprises comparing the run time length of one or more spare instruction slots with the run time length of a <u>conditional</u> code sequence associated with a corresponding portion of the initial instruction schedule.

Claim 8:

The method of claim 6, wherein evaluating the initial instruction schedule further comprises discarding <u>one or more conditional</u> code sequences having a run time length greater than the run time of one or more spare instruction slots associated with a corresponding portion of the initial instruction schedule.

Claim 9:

A computer program for performing correctness checks, the computer program being embodied on a computer-readable medium, the computer program comprising:

a first code segment configured to receive a set of instructions <u>comprising one or more</u>
<u>conditional code sequences that when executed direct one or more correctness checks</u>;

a second code segment configured to generate an initial instruction schedule and a
conditional instruction stream from the set of instructions, such that the initial instruction
schedule is devoid of <u>said conditional</u> code sequences ~~comprising correctness check functions~~
and such that the <u>conditional</u> code sequences of the conditional instruction stream are associated
with a corresponding set of one or more instructions in the initial instruction schedule;

a third code segment configured to evaluate the initial instruction schedule to determine
whether the initial instruction schedule includes spare instruction slots into which said
<u>conditional</u> code sequences ~~associated with correctness check function~~ can be inserted into the
initial instruction schedule such that a final instruction schedule would not require a longer run
time than the initial instruction schedule; and

a fourth code segment configured to insert <u>conditional</u> code sequences ~~associated with~~
~~correctness check function~~ into the spare instruction slots when sufficient spare instruction slots
exist in the initial instruction schedule to accommodate said <u>conditional</u> code sequences <u>in the</u>
<u>final instruction schedule</u>.

Claim 10:

The computer program of claim 9, wherein said second code segment generates a
conditional instruction stream comprising correctness check<u>s</u> ~~functions~~ that evaluate at least one
of a value, a range of values, and a relationship between values after execution of corresponding
instructions in the initial instruction schedule.

Claim 11:

The apparatus of claim 1, wherein said logic configured to evaluate the initial instruction schedule discards <u>one or more conditional</u> code sequences within the conditional instruction stream that ~~if~~ <u>when</u> inserted into a final instruction schedule would result in a final instruction schedule with a run time greater than a run time of the initial instruction schedule.

Claim 12:

The apparatus of claim 1, wherein said logic configured to evaluate the initial instruction schedule identifies <u>one or more conditional</u> code sequences within the conditional instruction stream for insertion into the initial instruction schedule.

Claim 13:

The apparatus of claim 12, wherein said logic configured to evaluate the initial instruction schedule identifies <u>one or more conditional</u> code sequences having a length that exceeds the length of a corresponding set of one or more spare instruction slots in the initial instruction schedule.

Claim 14:

The apparatus of claim 1, wherein said logic configured to generate the final instruction schedule inserts <u>one or more conditional</u> code sequences associated with correctness check<u>s</u> ~~functions~~ into spare instruction slots of the initial instruction schedule.

EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE

3.   Claims 1-15 are allowed.

The following is an examiner's statement of reasons for allowance.

The prior art of record, taken alone or in combination fails to teach or suggest the following claimed features:

A apparatus and method for performing correctness checks, comprising means and logic:
(i) for receiving a first set of instructions comprising conditional code sequences that when
executed would perform correctness checks; (ii) for generating an initial instruction schedule
devoid of said conditional code sequences and a conditional instruction stream comprising of one
or more of said conditional code sequences; (iii) for evaluating spare instruction slots in said
initial schedule so to insert therein said conditional code sequences in order to generate a final
instruction schedule that would not require a longer run time than the initial instruction schedule;
as recited in claims 1, 4, 6, and 9.

Hooker, USPN: 5,787,286, discloses identifying bubbles in the compiled code to insert
complex arithmetic tabulation and parametric measurement instructions but fails to
disclose/suggest a conditional code sequences purported to correctness checking included in the
first set of instructions as in (i) and generating therefrom a initial schedule devoid of such
conditional sequence and a conditional instruction stream to be used in conjunction with said
initial schedule as in (ii) to insert said conditional sequences therein based on the spare slots
evaluation as in (iii) to generate a final instruction schedule.

Austin, USPN: 5,644,709, teaches a memory error detection and computer performance
evaluation method, wherein memory boundaries checking code instructions are inserted but fails
to teach or render obvious receiving a first set of instructions comprising conditional code
sequences that when executed would perform correctness checks as in (i) and deriving a initial
instruction schedule devoid of said conditional code sequences which in conjunction with the
evaluation of empty slots in said schedule and inserting therein said conditional code sequences

from a conditional instruction stream as in (ii) enables the generation of a final schedule as in (iii).

Both Hooker and Austin teach inserting code into a compiled code but neither discloses or suggests starting with one or more conditional code sequences in the initial instruction set, deriving a conditional instruction stream from generating a initial instruction schedule based on said first instruction set; and use the spare slot evaluation to insert those conditional correctness checking instructions from said conditional instruction stream to generate an equal-length final instruction schedule.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (272) 272-3735. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571)272-3719.
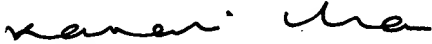
The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3735 (for non-official correspondence – please consult Examiner before using) or 703-872-9306 (for official correspondence) or redirected to customer service at 571-272-3609.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAT
December 17, 2000

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